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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,774	10/25/2005	Francois Droz	90500-000049/US	5249
30593 7590 05/04/2009 HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195			EXAMINER AYCHILLHUM, ANDARGIE M	
			ART UNIT 2841	PAPER NUMBER
			MAIL DATE 05/04/2009	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/529,774	Applicant(s) DROZ, FRANCOIS	
	Examiner ANDARGIE M. AYCHILLHUM	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/19/2008, 12/04/2008, 03/17/2008 and</u> | 6) <input type="checkbox"/> Other: _____ |
| <u>03/30/2005.</u> | |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Applicant's arguments filed 01/16/2009, with respect to Restriction Requirement have been fully considered and are persuasive. The restriction has been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 25-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodai (US 5,026,452) in view of Droz (US 2005/0085005 A1).

Pertaining to claim 25, Kodai discloses a method for manufacturing an electronic module (see column 3, lines 34-35) including at least two insulating sheets (4a and 4c, see fig. 5) defining its external faces, at least one element (2, see fig. 5) having a face flushing with an external surface of the module (see fig. 5) and,

comprising the steps of: placing at least one first insulating sheet (4c) including one window (40, see fig. 5) intended to lodge an element (2); inserting the element (2) into the window (40) of the first insulating sheet (4a); stacking an adhesive protection film (6) extending at least over a region between the element (2) and the edges of said window (40), said adhesive protection film (6) being coated or made up of an adhesive substance activated either at room temperature, or under the effect of heat and/or pressure, maintains the element (2) in said window (40); placing an electronic circuit in an area close to the window (40) containing the element (2), the adhesive protection film (40) and stacking a second insulating sheet (4c); and pressing or laminating the assembly previously formed.

But, Kodai does not teach an electronic circuit embedded between the two insulating sheets and does not provide filling material on the set formed by the first insulating sheet.

However, Droz teaches an electronic circuit (3, see figs. 2-6) embedded between the two insulating sheets (see figs. 2-6) and providing filling material (see paragraph [0014]) on the set formed by the first insulating sheet.

Therefore, it would be obvious to one having ordinary skill in the art at the time the invention was made to provide an electronic circuit embedded within the two insulating sheet and filling material formed by the first insulating sheet for an electronic module of Kodai based on the teaching of Droz. The motivation of filling material being to fill in the holes and compensate the surface relief due to the assembly of the different

elements of the module and also to provide a communication circuit in the circuit module that can transmit and receive signals.

Pertaining to claim 26, Kodai as modified by Droz further discloses the outline of the window (40 of Kodai) of the first insulating sheet (4a) adapts to the outline of the element (see Kodai fig. 5)

Pertaining to claim 27, Kodai as modified by Droz further discloses the element (2, see fig. 5 of Kodai) , lodged in the window (40 of Kodai), is thicker than the first insulating sheet (4a), and in that several insulating sheets (4a, 4c) are stacked, with the outlines of the windows of each sheet coinciding, and the total thickness of the stack being substantially equal to the thickness of the element lodged in the windows (40) of each sheet, the adhesive protection film (6 of Kodai) being placed on the stack by covering at least the outline of the window (40 of Kodai) of the last sheet of the stack.

Pertaining to claim 28, Kodai as modified by Droz further discloses the element (2, see Kodai fig. 2) lodged in the window (40 of Kodai), is thicker than the first insulating sheet (4a of Kodai) and in that the adhesive protection film (6 of Kodai) is placed on the element (2 of Kodai) in such a way as to also extend over the outline of the window of said first sheet, supplementary sheets (7, see Droz fig. 6) each provided with a window (40 of Kodai) are stacked, the outline of the windows of each sheet coinciding with the outline of the window of the first sheet (4a of Kodai), and the

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thickness of the assembly of sheets is substantially equal to the thickness of the element (2 of Kodai).

Pertaining to claim 29, Kodai as modified by Droz further discloses the element (2 of Kodai) inserted in the window (40 of Kodai) of the first insulating sheet (4a of Kodai) is made up of an electronic component (see fig. 2) connected to the electronic circuit (3, see Droz fig. 3).

Pertaining to claim 30, Kodai as modified by Droz further discloses the element (2 of Kodai) having a first face flushing with the external surface of the module (see fig. 5 of Kodai) and a second face presenting conductive connection areas (2a of Kodai), comprising a step of connection of the conductive connection areas (2a of Kodai) of the element (2) to the electronic circuit (3 of Droz) succeeding the step of placement of the electronic circuit (3 of Droz).

Pertaining to claims 31, 32 and 36, Kodai as modified by Droz further discloses prior providing the filling material (see paragraph [0014] of Droz), a step of placing conductive connection areas (2a of Kodai) on the internal face of the element (2 of Kodai) opposed to the face flushing with the external surface of the module, said conductive connections areas (2a of Kodai) being then connected to the electronic circuit (3 of Droz).

Pertaining to claim 33, Kodai as modified by Droz further discloses prior to the application of the adhesive protection film (6 of Kodai) on the assembly formed by the first insulating sheet (4a of Kodai) and the element (2, see Kodai fig. 5), the electronic circuit (3, see Droz figs. 2-5) is placed on said adhesive protection film (6 of Kodai) and the assembly formed by the protection film (6 of Kodai) and the electronic circuit (3 of Droz) is applied onto the assembly formed by the first insulating sheet (4a of Kodai) and the element (2 of Kodai).

Pertaining to claim 34, Kodai as modified by Droz further discloses the adhesive protection film (6) includes at least one window (40) facing the conductive connection areas (2a of Droz) of the element (2 of Kodai).

Pertaining to claim 35, Kodai as modified by Droz further discloses the element (2 of Kodai) inserted in the window (40 of Kodai) of the first insulating sheet (4a) is constituted by an inert core (see fig. 5 of Kodai) intended to be removed at the end of the module manufacturing process, leaving a cavity having the shape of the core (see fig. 5 of Kodai) previously inserted on one of the faces of said module, said cavity being used for a subsequent insertion of a fixed or removable electronic component (3 of Droz).

Pertaining to claim 37, Kodai as modified by Droz further discloses the electronic circuit (3 of Droz) includes connections ending on the internal face of the element opposed to the face flushing with the external face of the module (see fig. of

Kodai), said connections forming conductive connection areas (2a of Droz) at the bottom of the cavity when the element (2 of Kodai) is removed.

Pertaining to claim 38, Kodai as modified by Droz further discloses the adhesive protection film (6 of Kodai) includes at least one window (40) facing the connection areas of the element (2, see Kodai fig. 5).

Pertaining to claim 39, Kodai as modified by Droz further discloses the first insulating sheet (4a of Kodai) includes a cavity (40 of Droz), the outline of said cavity (40 of Droz) adapting to the outline of the electronic circuit placed in said cavity (40, see Kodai fig. 5).

Pertaining to claim 40, Kodai as modified by Droz further discloses an assembly of at least two insulating sheets (4a and 4c, see fig. 5) and at least one element, a first insulating sheet (4c) defining one of the faces of the module including at least one window (40, see fig. 5) in which the element (2) is lodged, one face of said element flushing with the external surface of said first sheet the second insulating sheet (4c) constituting the other face of the module (see fig. 5); the two insulating sheets (4a, 4c); and an adhesive protection film extending over a region covering at least the outline of the window in which is lodged the element (2) and situated between the first insulating sheet (4a).

But, Kodai does not teach an electronic circuit embedded between the two insulating sheets and does not provide filling material on the set formed by the first insulating sheet.

However, Droz teaches an electronic circuit (3, see figs. 2-6) embedded between the two insulating sheets (see figs. 2-6) and providing filling material (see paragraph [0014]) on the set formed by the first insulating sheet.

Therefore, it would be obvious to one having ordinary skill in the art at the time the invention was made to provide an electronic circuit embedded within the two insulating sheet and filling material formed by the first insulating sheet for an electronic module of Kodai based on the teaching of Droz. The motivation of filling material being to fill in the holes and compensate the surface relief due to the assembly of the different elements of the module and also to provide a communication circuit in the circuit module that can transmit and receive signals.

Pertaining to claim 41, Kodai as modified by Droz further discloses the internal face of the element (2) opposed to the face flushing with the external surface of the module (see fig. 5) includes conductive connection areas (2a of Kodai) connected to the electronic circuit (3, see Droz fig. 3).

Pertaining to claim 42, Kodai as modified by Droz further discloses wherein the adhesive protection film (40 of Kodai) includes at least one window facing the conductive connection areas (2a of Kodai) of the element (2 of Kodai)

Pertaining to claim 43, Kodai as modified by Droz further discloses the external faces of the insulating sheets (see fig. 5 of Kodai) constituting the external faces of the module include a decoration or a marking (see fig. 5 of Kodai)

Pertaining to claim 44, Kodai as modified by Droz further discloses wherein the element (2, see fig. 5 of Kodai) inserted in the window of the first insulating sheet (4a of Kodai) is constituted by an inert core intended to be removed leaving a cavity (see fig. 5 of Kodai) having the shape of the core on one of the faces of said module, said cavity being made to be used for the subsequent insertion of a fixed or removable electronic component (see fig. 2 of Kodai).

Pertaining to claim 45, Kodai as modified by Droz further discloses the bottom of the resulting cavity (see fig. 5 of Kodai), after the element (2 of Kodai) has been removed, includes conductive connection areas connected to the electronic circuit (3, see figs. 2-6 of Kodai).

Pertaining to claim 46, Kodai as modified by Droz further discloses the element (2 of Kodai) is constituted by an electronic component (see fig. 2 of Kodai).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDARGIE M. AYCHILLHUM whose telephone number is (571) 270-1607. The examiner can normally be reached on (Mon-Fri from 8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean A. Reichard/
Supervisory Patent Examiner, Art
Unit 2841

A.A.
April 11, 2009